PIP-II LLRF Station and Multi-Frequency RF System Status

Ed Cullerton
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PXIE Hardware (PIP-II LLRF Station Test system)

• 4-Channel Upconverters
  • Prototype stage

• 8 Channel Receivers
  • Upgrade to existing 8-channel receivers

• Receiver Temperature Control Unit
  • Prototype stage

• Master Oscillator
  • Assembly in Progress

• SOC-MFC FPGA Controller
  • Prototype stage
PXIE LLRF System
Back of PXIE LLRF Racks
PXIE Prototype RF Hardware in the Lab
PXIE/PIP-II RF Station Hardware Status

• All RF hardware schematic design done
• All RF chassis design done
• 80% done with Board layout
• Lab Prototyping in progress
SOC-MFC FPGA Controller
SOC-MFC FPGA Controller Status

- Linux is now running on the system
- Development system is on the controls network for testing and integration
- Working with controls to integrate Erlang frontend
- Analog interfaces currently being tested
- Cleaning up FPGA development code before moving to production version
- On-board devices communicate with both Linux and FPGA
- Rev 2 board layout complete and in review.
PIP II Multi-Frequency RF System Overview

- 4 phase averaged reference lines in the tunnel.
  - 162.5, 325, 650, and 1300 MHz sections.
- 1 phase averaged 1300 MHz line upstairs.
- 162.5 MHz Low Phase Noise Crystal Master Oscillator.
- Frequency doublers at the end of each section to provide the next section source.
- 4 Cavities per LLRF FPGA/Station.
PIP-II Distribution System

PIP-II RF Phase Reference System

Phase Averaging 1300 MHz Distribution

1300 MHz Temperature Controlled Master Oscillator
- 162.5 MHz Reference Signals
- 1300 MHz Reference Signals
- 1320.3 MHz FPGA CLOCK
- 182.8 MHz L.O.
- 162.5 MHz Oscillator
- Timing Clocks
- Booster/MEBT Chopper

To Booster Timing

325.0 MHz Temperature Controlled Distribution
- 325.0 MHz Temperature Controlled Distribution
- (x2) 325.0 MHz Reference Signals
- Phase Averaging Reference Line

650.0 MHz Temperature Controlled Distribution
- 650.0 MHz Temperature Controlled Distribution
- (x2) 650.0 MHz Reference Signals
- Phase Averaging Reference Line

1300 MHz Temperature Controlled Distribution
- 1300 MHz Temperature Controlled Distribution
- (x2) 1300 MHz Reference Signals
- Phase Averaging Reference Line

LLRF FPGA
- UP-CONVERTERS/DOWN/CONVERTERS
- INSTRUMENTATION
Phase Averaging Reference Line at ASTA

* changes in cables lengths between tap positions due to temperature changes ($L = L + \Delta L$)
the output becomes: $\text{OUT} = A_c \cos (wt + \phi_f + \Delta \phi_f) + A_s \cos (wt + \phi_s - \Delta \phi_s)$

When the phase at the shorted end of the reference line is held constant, $\Delta \phi_s = -\Delta \phi_f$

When $\Delta \phi = -\Delta \phi_f$
arg $\{ A_c \cos (wt + \phi_f + \Delta \phi_f) + A_s \cos (wt + \phi_s - \Delta \phi_s)\} = \text{arg} \{ A_c \cos (wt + \phi_f) + A_s \cos (wt + \phi_s)\}$
Multi-frequency RF System
162.5 MHz Frequency Source
Temperature Controller Rack
PIP-II Multi-Frequency RF system Status

- Part selection in Progress
- 325 MHz “Slave Oscillator” schematic design complete