200 Ohm MEBT Chopper Development Progress

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PIP-II Meeting

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Topics

- Helix assembly and test results
  - Alex Chen - mechanical and design, thermal analysis
  - 3D modelling results – Mohamed Hassan
  - Electrical time domain performance
- Progress with 500 V driver
  - On-going cascode switch results
  - LDRD alternative
- Conclusions
Helix Requirements

- Critical parameters
  - Traveling wave propagation velocity
    - Must match beam $\beta = 0.0667$ to $<1\%$
  - Impedance
    - Helix and load are impedance matched to $\sim5\%$
  - Dispersion
    - Less than 5% effect on beam
  - Power handling per each helix
    - Average power dissipation calculated to be 6 – 8 Watts with 200 Ω load at 35 MHz average switching rate
    - Specified to handle absorption of 40 Watts beam power
Helix Assembly

- One Helix built - Alex Chen’s mechanical design
  - Machined copper ground tube with water cooling
  - Stepped ends for better impedance match
  - High thermal conductivity ceramic spacers (4)
  - Vacuum compatible epoxy used at all ceramic-to-copper spacer interfaces
  - Fixture used to locate electrodes when laser-welded to each wire
  - All supports are ceramic
  - Design includes beam aperture restrictions
Helix Assembly

- Welded Electrodes
- Tube Is Stepped At Both Ends
- High Thermal Conductivity Ceramic Spacers (4). Notched For Each Wire Crossing
- All Ceramic-To-Copper Interfaces Are Epoxied for better thermal transfer
Residual Gas Analysis (RGA) results (1)

- Residual gases are Hydrogen, Water, and Air
- Hydrocarbons are very low
• Outgas due to electrical heating is insignificant
Temperature Rise (°F) (in air)

- Water Cooled
- Water Off, Power on
- Water @85°F
- ~4 °F rise
- ~50 °F rise above air
- Room @67°F

- Majority of power is conducted through the ceramic to water
Temperature Rise (°F) (in vacuum)

- 17 °F wire temperature rise with 40 Watts applied
Mohamed and I worked to resolve differences between model and bench test of actual helix.

Same approach used for critical measurements of both bench test and 3D model:

- Pulse edge of the transmitted voltage used to measure beta
- Reflection of pulse flattop used to determine helix Zo

Result: very close agreement:

<table>
<thead>
<tr>
<th></th>
<th>Target</th>
<th>Measured</th>
<th>3D Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zo</td>
<td>200</td>
<td>~185</td>
<td>189</td>
</tr>
<tr>
<td>β</td>
<td>0.0667</td>
<td>0.0633</td>
<td>0.0634</td>
</tr>
</tbody>
</table>

3D modelling can be used to adjust the helix to proper beta.
Helix – Complete 200 Ω System Electrical Test

- Best evaluation method is with time domain using applied pulses
  - Re-reflections at the output reveal errors
    - Helix end effect impedance mismatch
    - Mismatch between all joining sections
    - Helix-to-load mismatch
  - Helix dispersion readily evident on the transmitted voltage
ASSEMBLED FOR ELECTRICAL TESTS

Load side feed-through

200 Ω microstrip line

Zero Volt image plane
Helix – Feed-Through Connections

Driver End

Vacuum Side

Air Side

Load End

Vacuum Side

Water cooling line
Helix Electrical Test – Best Match, Low Power Resistor Load

- Re-reflections reveal all impedance mismatches
- Generator rise time = 1.5 ns
- No mismatch compensation yet applied
- Dispersive beam effects are ½ that shown
- Stepped-ends reduced helix mismatch end effects

Transmitted Voltage

Dispersion effects

Helix end effects + all line mismatches

5% error limit
Helix Complete Assembly – High Power Load

- Yellow – input signal
- Violet – transmitted voltage at the load
- Helix-to-load impedance mismatch is evident
- All other mismatches <5%

Helix end effects + all line mismatches

185-to-200 Ω mismatch

5% error limit
Progress with 500 V driver
Driver – 500 V Low-Side Switch Topology

- 5 stages operated at 2 MHz CW
- 4 stage version operated 22 MHz CW
- These CW limits caused by AC power distribution issue that can be easily resolved
- This effort halted during burst and CW testing

5-stage cascode switch assembly

200 Ω load
Driver – 500 Volt Switch

2.3 ns fall time, 
~9 ns rise time (5-95%)

Cascode, low-side switch topology

200 OHM ATTEN.

0 V

3.5ns Flattop

-500 V

15ns Flattop
Driver – Cascode Switch Development Work

- SPICE circuit modeling effectively employed
  - Good GaN FET models obtained from Polyfet Devices Inc.
  - Models included measured PCB parasitics
  - Cascode model performance matched bench tests

- Spice modelling of the 5-stage bipolar switch indicated degraded performance in rise time and voltage sharing. Thus did not meet specifications.

- Effort shifted away from the cascode switch
Driver - Alternative Scheme

- In the development process it was determined that a single driver chain has very low jitter (~60ps). Because of this, one can consider driving all series switches individually with suitable isolation.

- Advantages to multiple stages driven individually
  - One switch each drives each helix
    - A high-side and a low-side
  - No bipolar switch needed
    - No dead time that “eats” up 2 ns during transitions

- A number of schemes are commonly used
  - Our speed requirement reduces the options to a unique approach

- Meanwhile, GaN FETs available by July from GaN System Inc.
  - 650 V rated (currently using 200 V rated parts)
  - Fewer than 5 stages would be required
  - A modified driver PCB required
    - Same driver circuit, only GaN FET footprint is different
Alternative Scheme – LDRD

- My LDRD proposal to develop a GaN FET driver was accepted to pursue an individually-driven approach
- Effort thus far accomplished
  - Used SPICE to design a new GaN FET driver board
    • Capable of driving higher capacitance GaN FETs
    • More efficient
    • Transformers used to communicate triggers to each board
  - PCBs laid out and on hand, with parts
  - Currently matching the timing of two boards to drive simultaneously
  - Pursued use of laser/photodiode as free-space communication link for better isolation than transformers (and simpler circuitry?)
    • Developed fast laser transmitter and detector receiver circuits
    • Evaluated multiple lasers and photodiodes in combination
Conclusions

- **Helix**
  - Impedance mismatches between sections are unmeasurable
    - Stepped-ends reduced helix mismatch end-effects
  - 3D modelling will be used further
    - Helix E-field kicker efficiency
    - Determine the helix dimensions of the next, “final”, helix
    - Will lowering Zo from 200 Ω help lower dispersion?
  - Out-gassing is not a concern
  - Ceramic spacers very effective in heat transfer

- **Driver development**
  - Cascode switch work has been suspended
  - Effort will be to develop a driver with LDRD resources
    - Specifications are defined following PIP-II requirements
  - Laser/photodiode free-space communication option is an option should transformers prove problematic
Reasons for helix geometry errors

- Dimensions chosen before improved beta measurement technique
- Ceramic spacer dielectric higher than vendor’s stated value
  - Technical division measured various ceramics and determined real value
- Previous prototype used ceramics having different dielectric constant
Factors, in combination, halted the cascode switch development

1) Parasitics degrade performance and increase with the number of states
   - Parasitics capacitance to ground
   - Inductance, especially lead length through the switch

2) 5 stages required for 500 V - using the Polyfet Devices Inc. GaN FETs

3) Cascode switch topology requires bipolar topology
   - Bipolar switch topology requires dead time during each edge (~2ns)
   - Circuit capacitance is double that of single low- or high-side switch
     - High circuit capacitance means higher current during the rise/falling edges