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PIP-II Injector LLRF Update

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PIP-II Meeting

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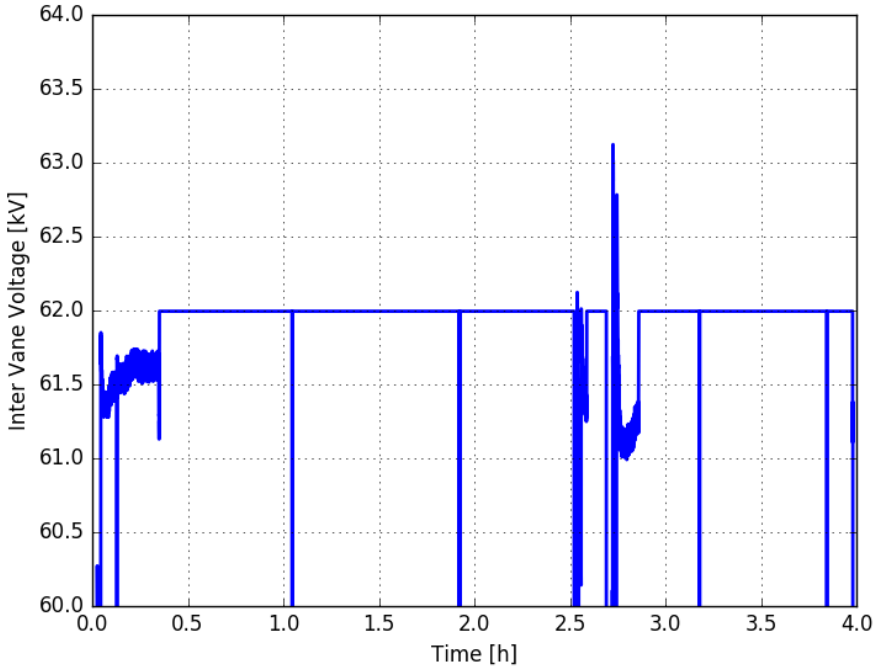
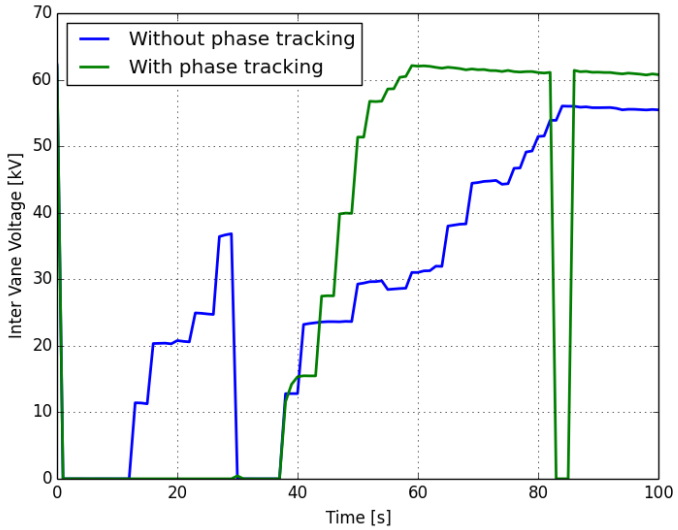
LLRF Update:

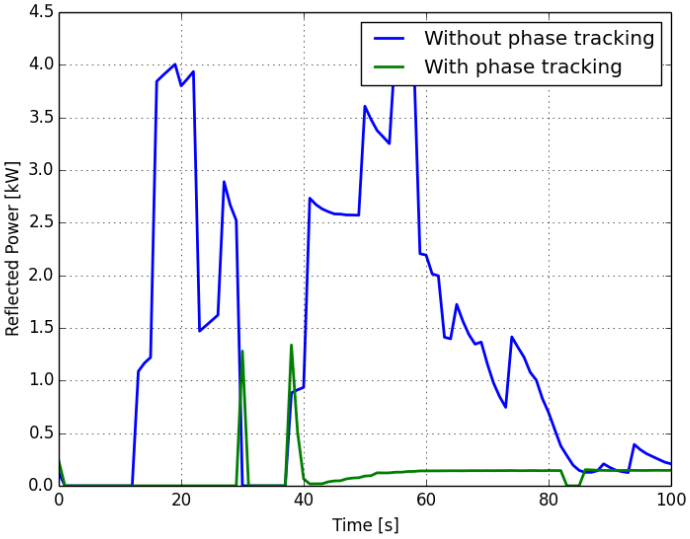
- System status
  - Conditioned to 62kV CW (Some conditioning to 65kV was done, not yet stable at the higher field)
  - Stable operation in GDR at 162.5 MHz with some manual resonance control (Auralee is working on automatic resonance control)
  - Manual trip recovery is 5-10 minutes for “big trips”
  - Small trips recover automatically
  - Pulsed operation, still 5ms at 10Hz, new boards are in development
  - Working with timing to fix RF-to-beam jitter
- Recently implemented changes in the LLRF system
  - Increase frequency tracking gain for better performance
  - Added phase tracking loop to compensate for drift in the high power system when in self excited loop



LLRF Phase tracking loop

- After a big trip we need to drop into self excited loop
- Fast changes in temperature in going from full power at CW to off cause the phase of the high power RF system to drift, this drift is bad for our frequency tracking loop
- Before implementing the phase compensation loop this drift needed to be compensated for manually resulting in slower recovery time when ramping the RF power
- Top: Inter vane voltage with and without phase tracking during trip recovery
- Bottom: Average reflected power with and without phase tracking during trip recovery

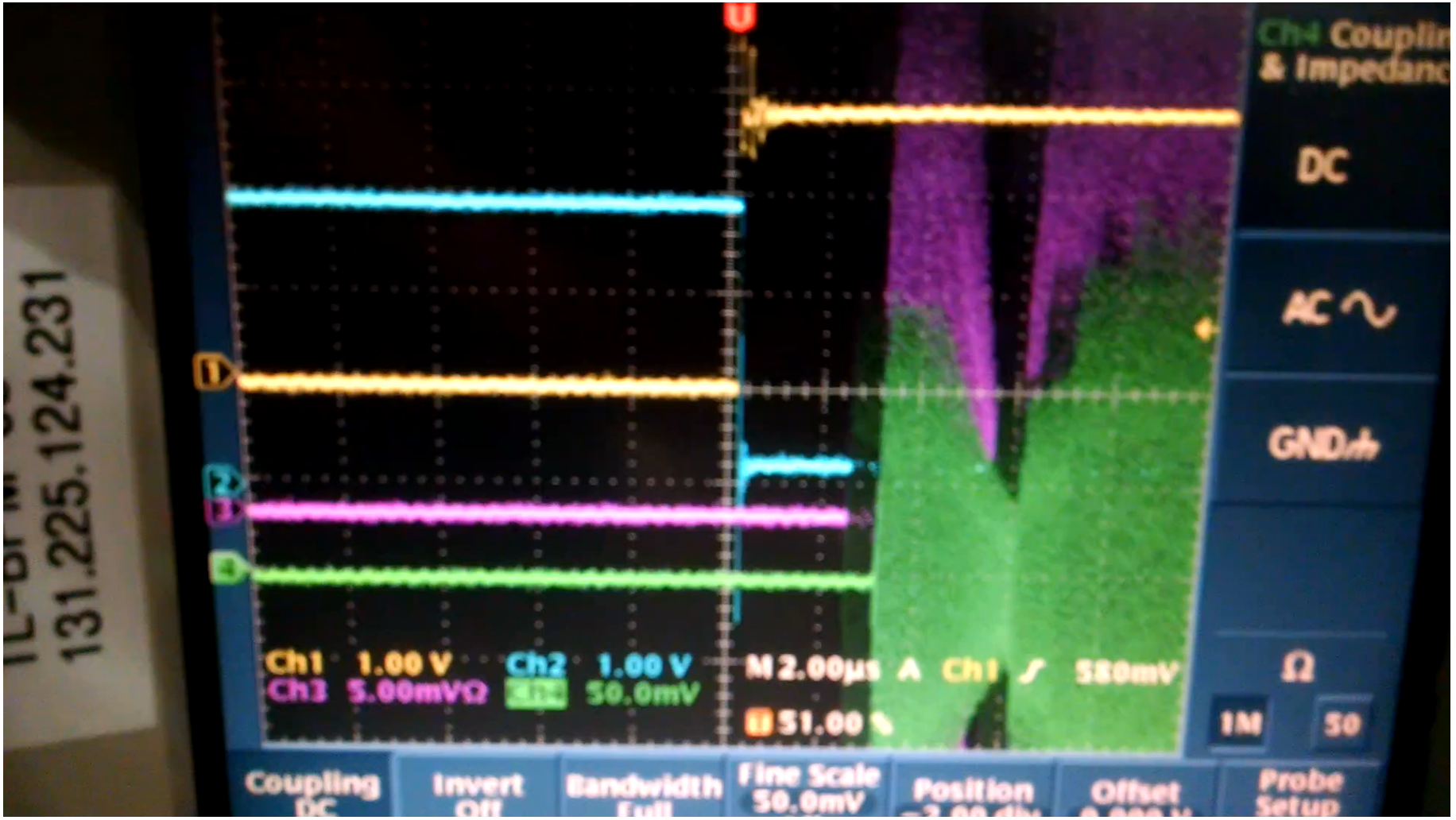




Timing jitter

- We were experiencing large timing jitter between the RF and the beam greater then 1 microsecond
- After some investigation we found an issue with the way we were triggering the RF to turn on in the firmware
- This was corrected which reduced the jitter, but there is still a residual 300-500 ns jitter between the RF and the beam
  - Mike Kucera measures 50 to 70 ns
- Adaptive beam compensation algorithms are sensitive to jitter. An algorithm that is not sensitive to jitter would be too computationally intensive to make pulse-to-pulse corrections

Scope trace showing timing jitter



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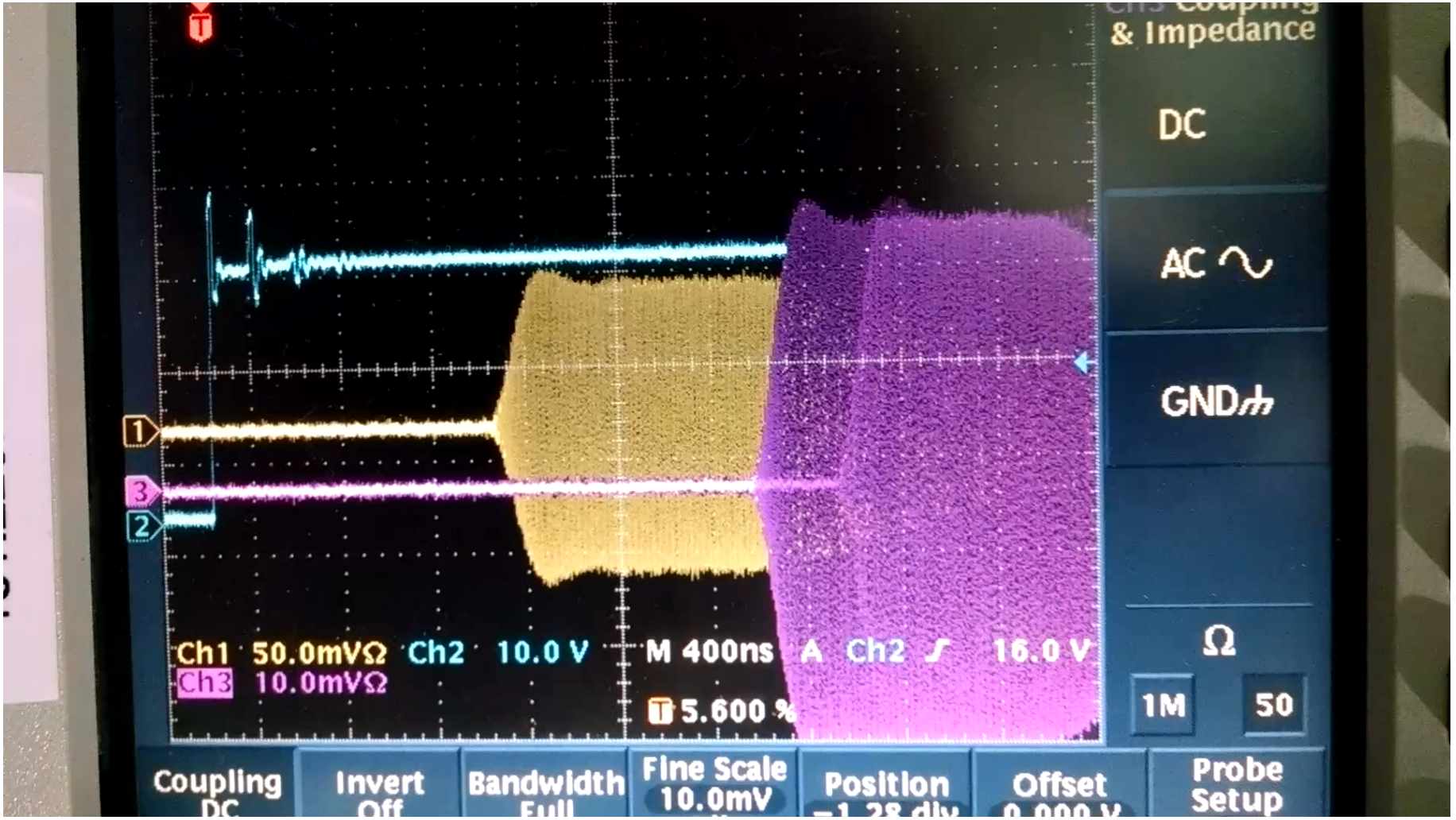
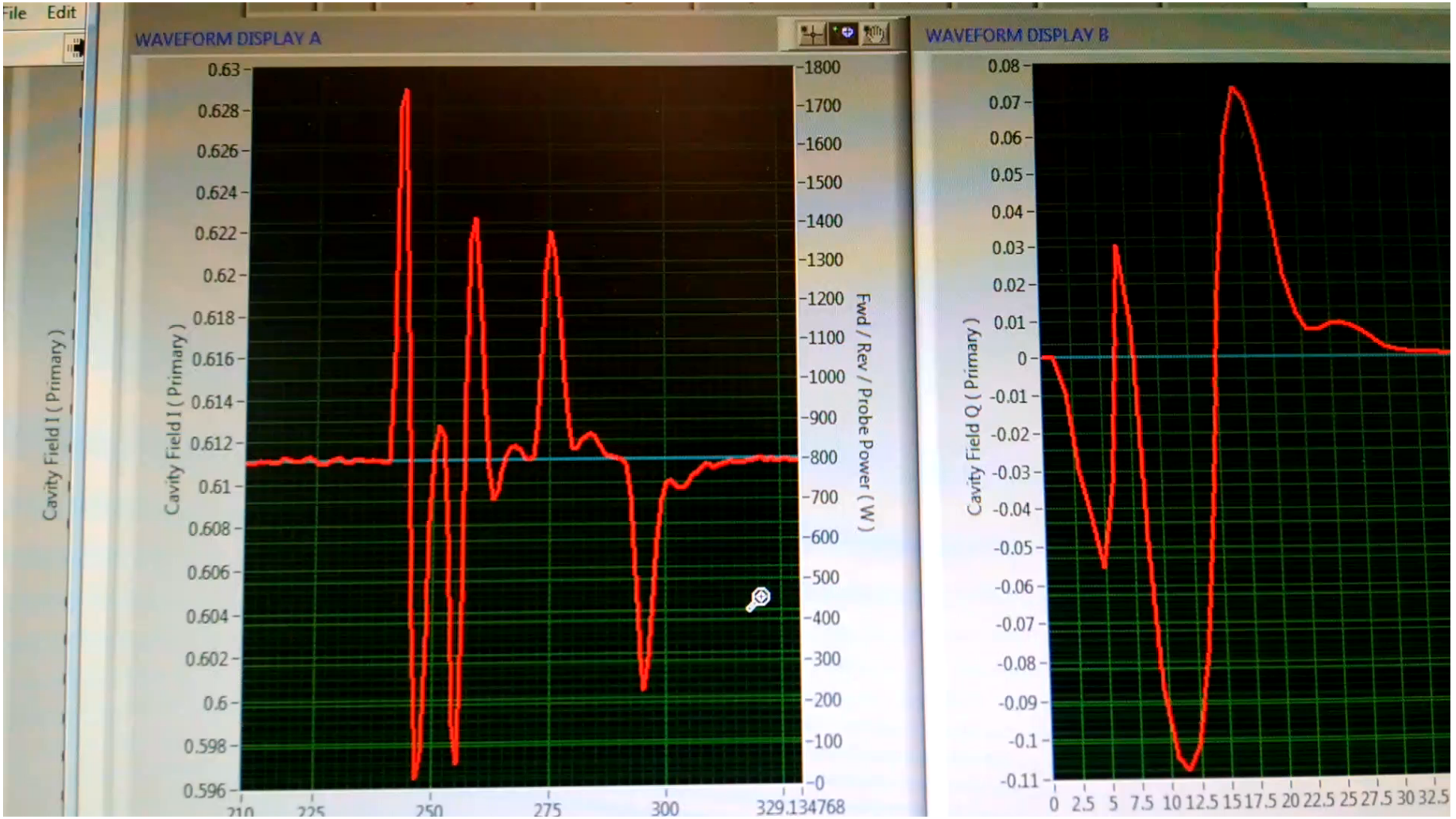
Scope trace from after fixing jitter in Buncher firmware



Jitter between buncher and beam still present in RF signals



Resolving timing jitter

- The timing jitter presents a significant limitation for the adaptive beam compensation
- We have fixed the jitter between the timing system and the LLRF system, but there is still jitter between the beam and LLRF
- Currently the adaptive beam compensation can correct for changes in current, but not for changes in beam phase
- More work needs to be done in order to correct for this jitter

Phase-flips

- There was an issue with one of the I/Q modulators on the prototype up-converter which introduced an extra divide by two in the LO that was causing a random 180 deg. phase-flip between the two RF amplifiers when the crate is power cycled

- Rev-B up-converter fix this issue and will be installed shortly

LLRF for Buncher 2 & 3

- The current controller cards used for the RFQ and Buncher cavity have obsolete components, the FPGA is not no longer supported by Altera and we have no more cards available
- A newer version ‘SOC-MFC’ has been built and is being programmed for LCLS-II cryomodule testing at CMTS.
- When that is complete we will use them to upgrade systems at PIP-II injector. We are also changing RF hardware to support the PIP-II IF frequency of 20 MHz.

LLRF Upgrade to support Buncher 2 & 3

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Fermilab PXIE LLRF Racks

PIP-II Injector LLRF Station Controller Upgrade

- New bus architecture
- Streamlined DAQ and Controller architecture
- Integrated front-end ARM processor (HPS)
- Leverages CMTS development work