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Hardware for the Microphonics Control Test Stand

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PIP-II Weekly Meeting

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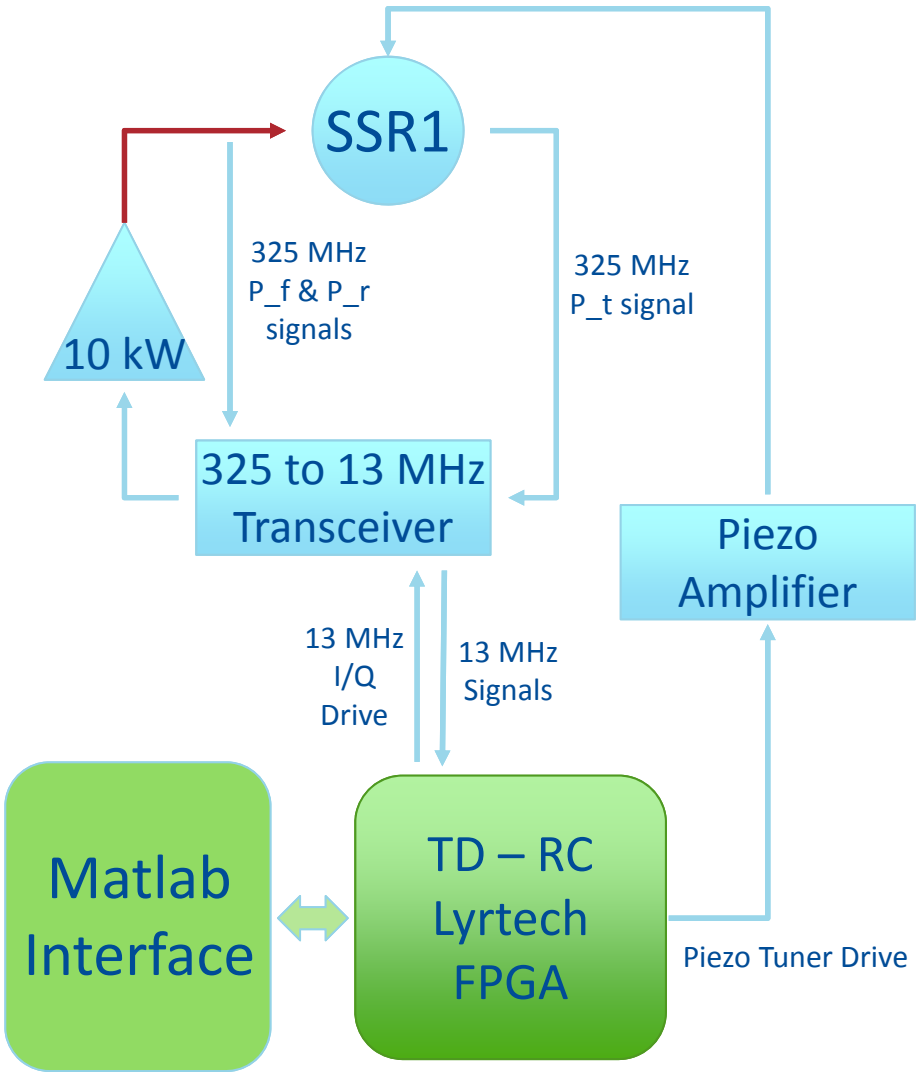
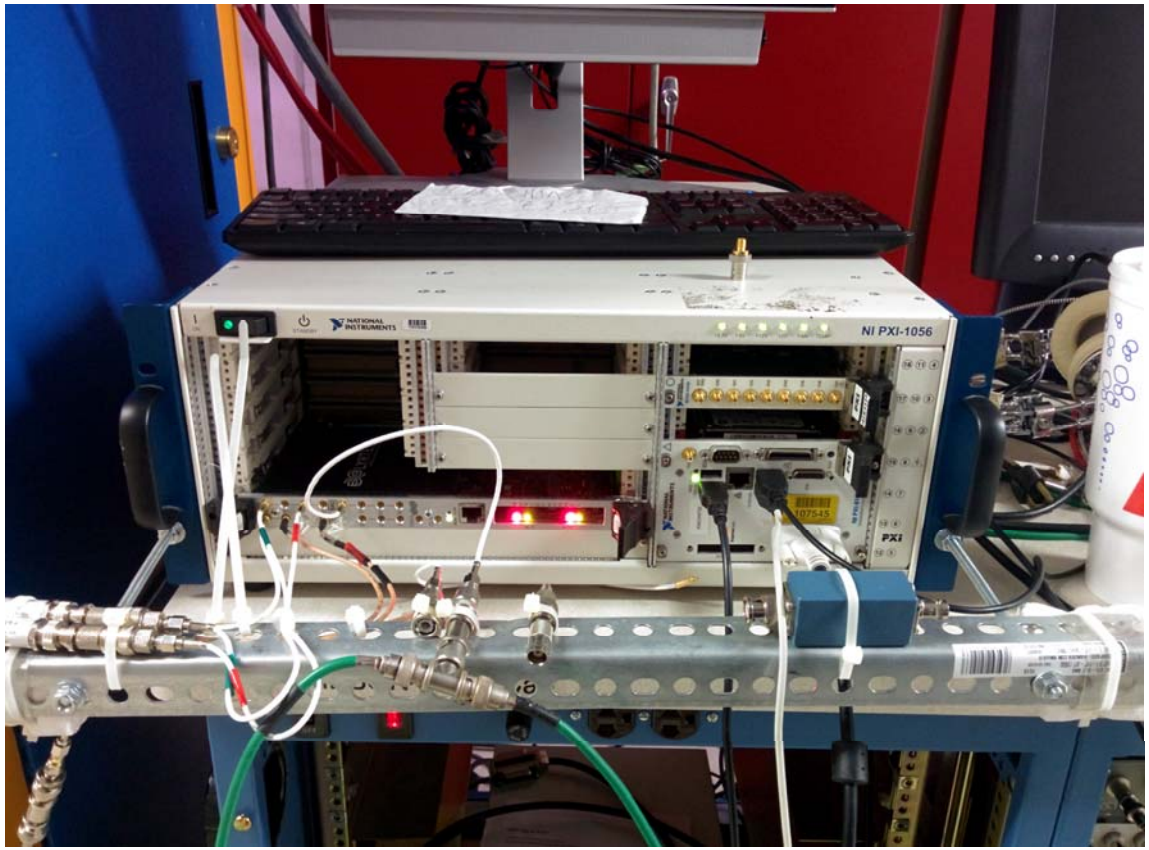
Resonance Control System - Overview

- Compensation system controls cavity drive and tuner
- FPGA generates drive @ 13 MHZ
- AD-LLRF Transceiver upconverts
- HLRF Amplification
- Cavity Responds
- Forward, Reverse, and Probe signals are captured, downconverted, and monitored by FPGA
- FPGA also generates piezo tuner signal
- Matlab controller allows setting FPGA registers and recording signals for offline processing



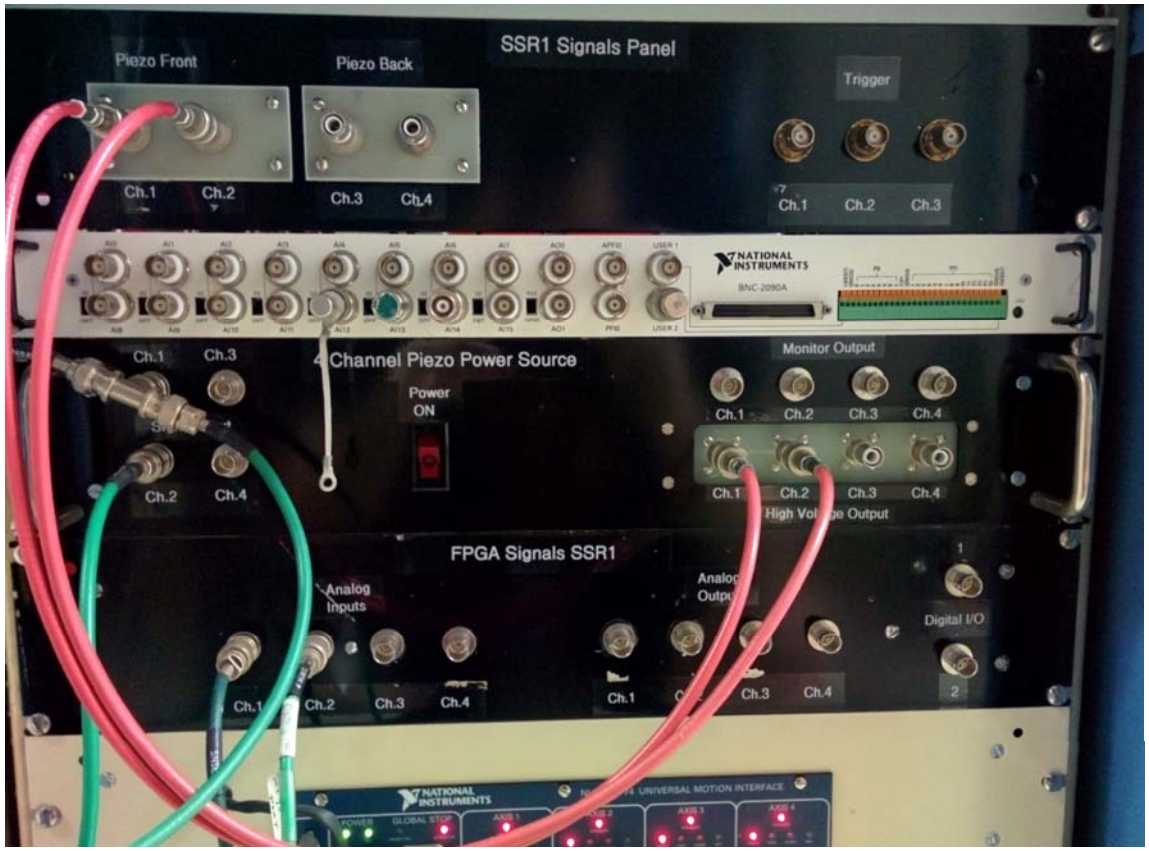
FPGA Details

- Xilinx Vertex IV SX-55
- 512 internal multipliers
- 104 MHz clock speed
  - 13 MHz RF x 8
- 8 Channel ADC/DACs
  - 14 bit
- Matlab/VHDL code written in house
- NI PXI Crate
  - Local Controller for Matlab Interface



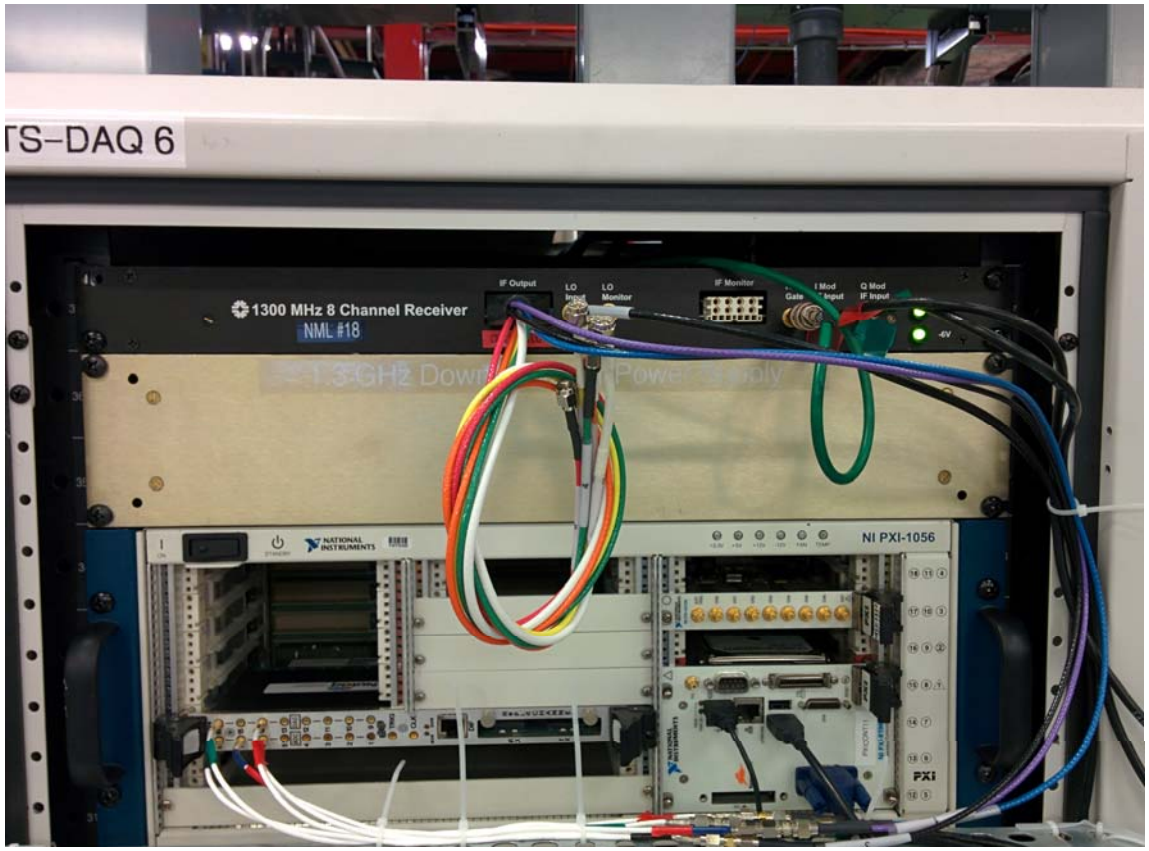
Piezo Amplifier

- DC amplifier with gain of ~20
- Built around a PiezoMaster amplifier
- Crate made in-house (cheap, but probably not optimally quiet)



AD-LLRF Transceiver

- Eight channel up/down conversion
- Designed for single sideband mixing of f and f + 13 MHz with a bandwidth of a couple MHz on the drive
- Not wide enough bandwidth for all nine ILC cavity modes, for instance
- Input/Outputs and Monitor ports

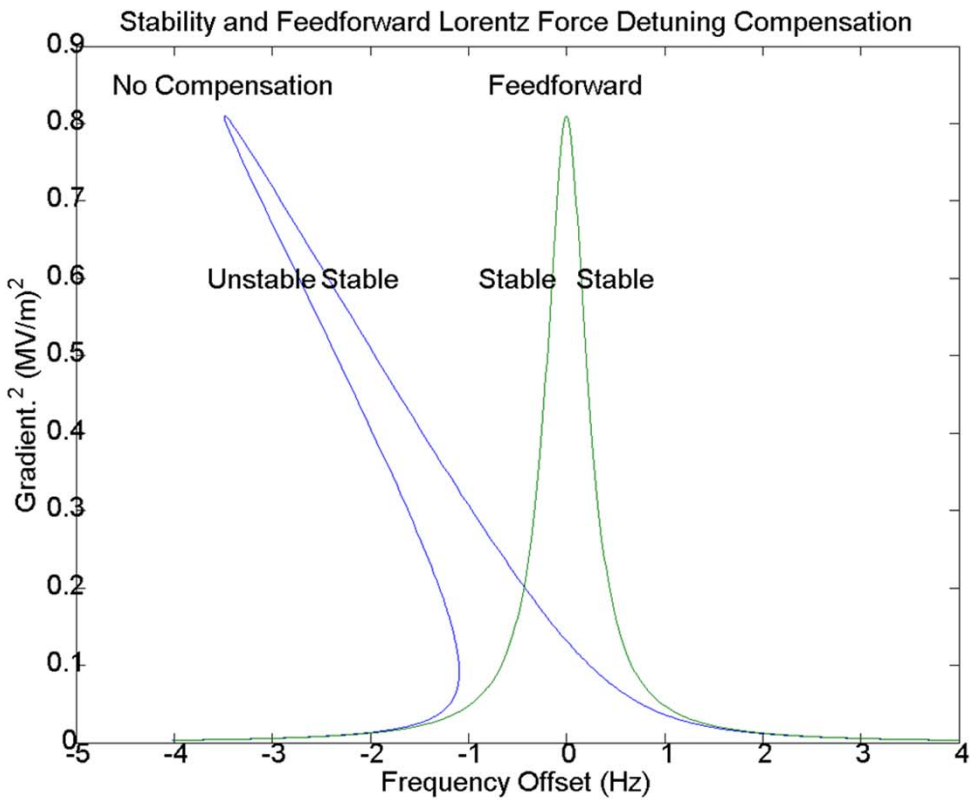


FPGA Firmware Features

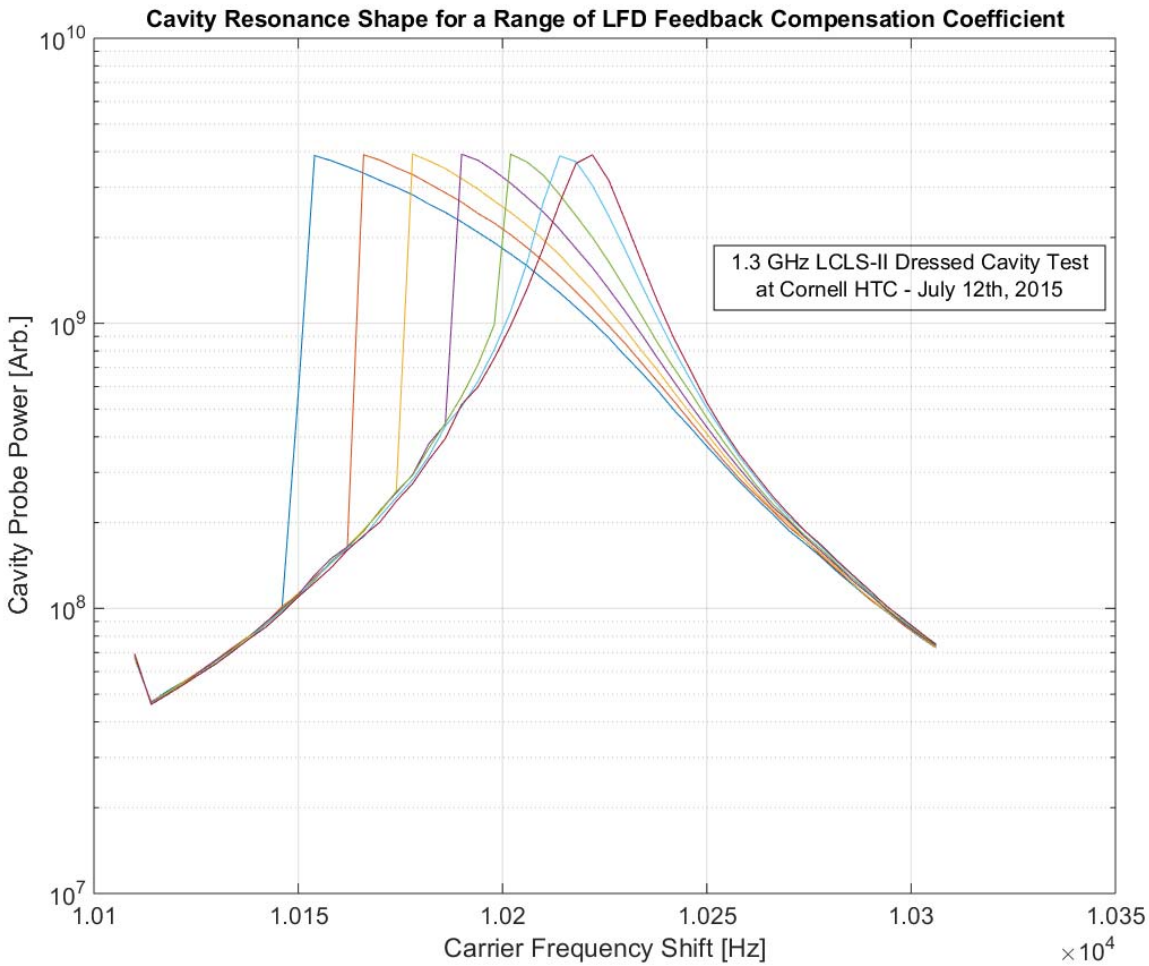
- Most of the work is focused on the FPGA firmware
  - Forward, Reverse, and Probe power are digitized, then digitally downconverted to baseband
  - Features:
    - Numerically Controlled Oscillators
    - Gains/Rotations (Signal Calibration)
    - Mixing, filtering
    - Lorentz Force Compensation (proportional to E^2)
    - Detuning Compensation (proportional to detuning)
    - Phase Lock Loop
  - Drive is generally open loop, fixed amplitude and frequency, but doesn't have to be

Lorentz Force Compensation

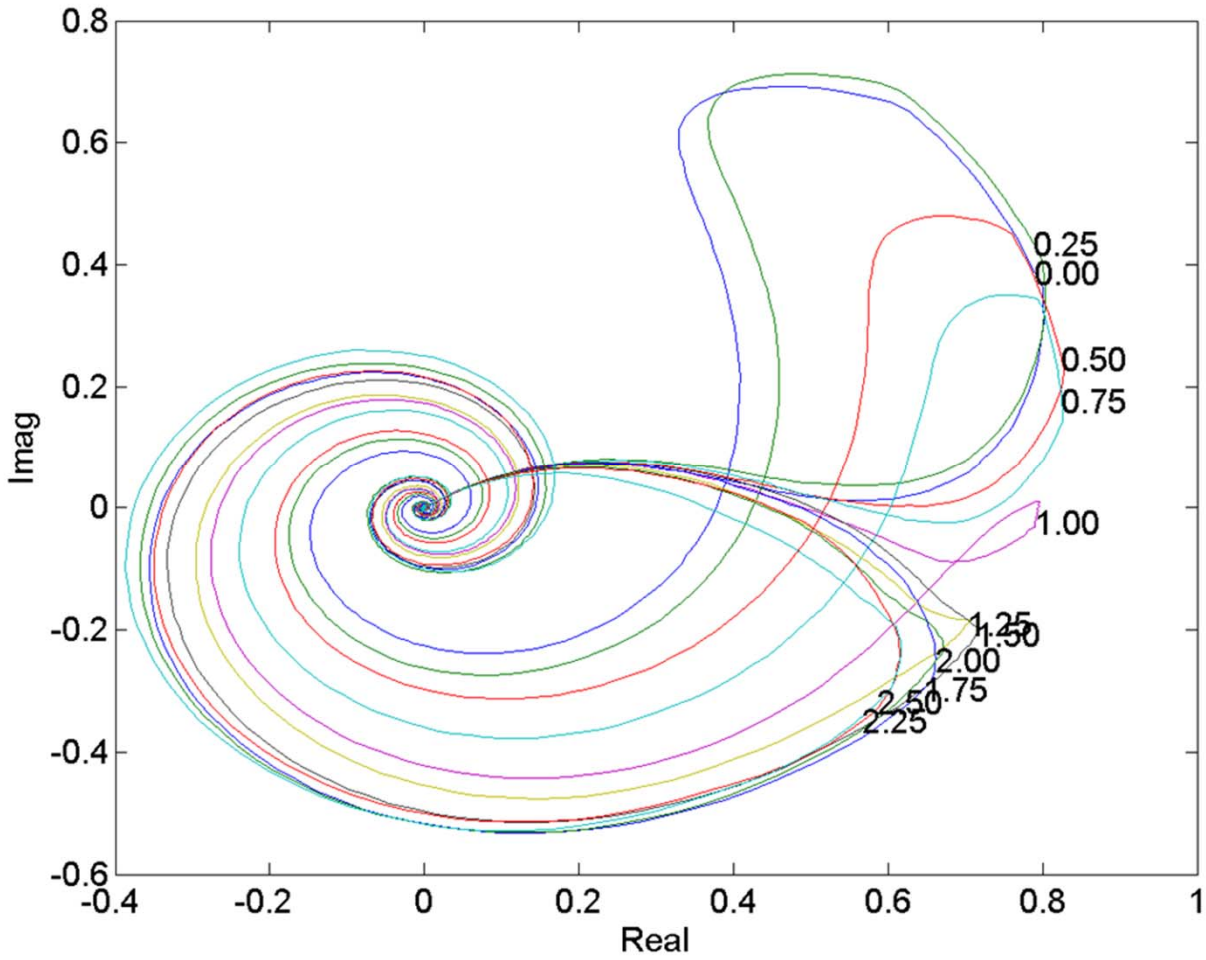
- There is a detuning of the cavity from the internal radiation pressure of the fields
- This is proportional to stored energy (E^2)
- E^2 is calculated on the fly and proportionally fed into the piezo to cancel this shift



CW Lorentz Force Compensation

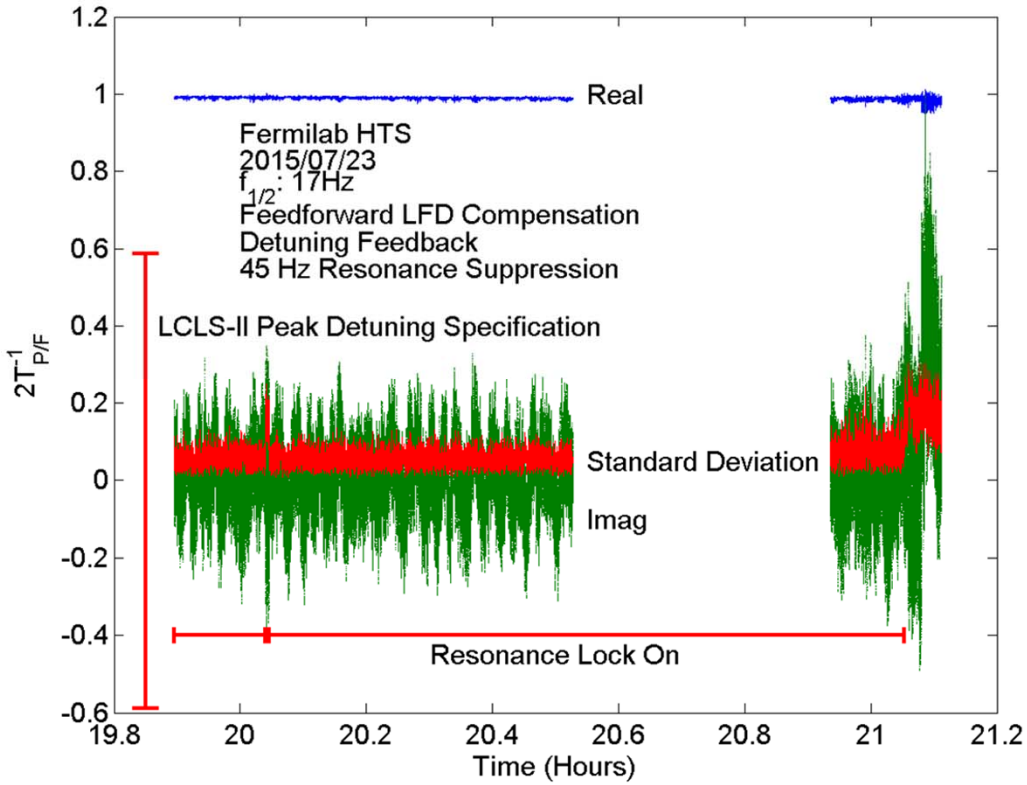


Pulsed Lorentz Force Compensation

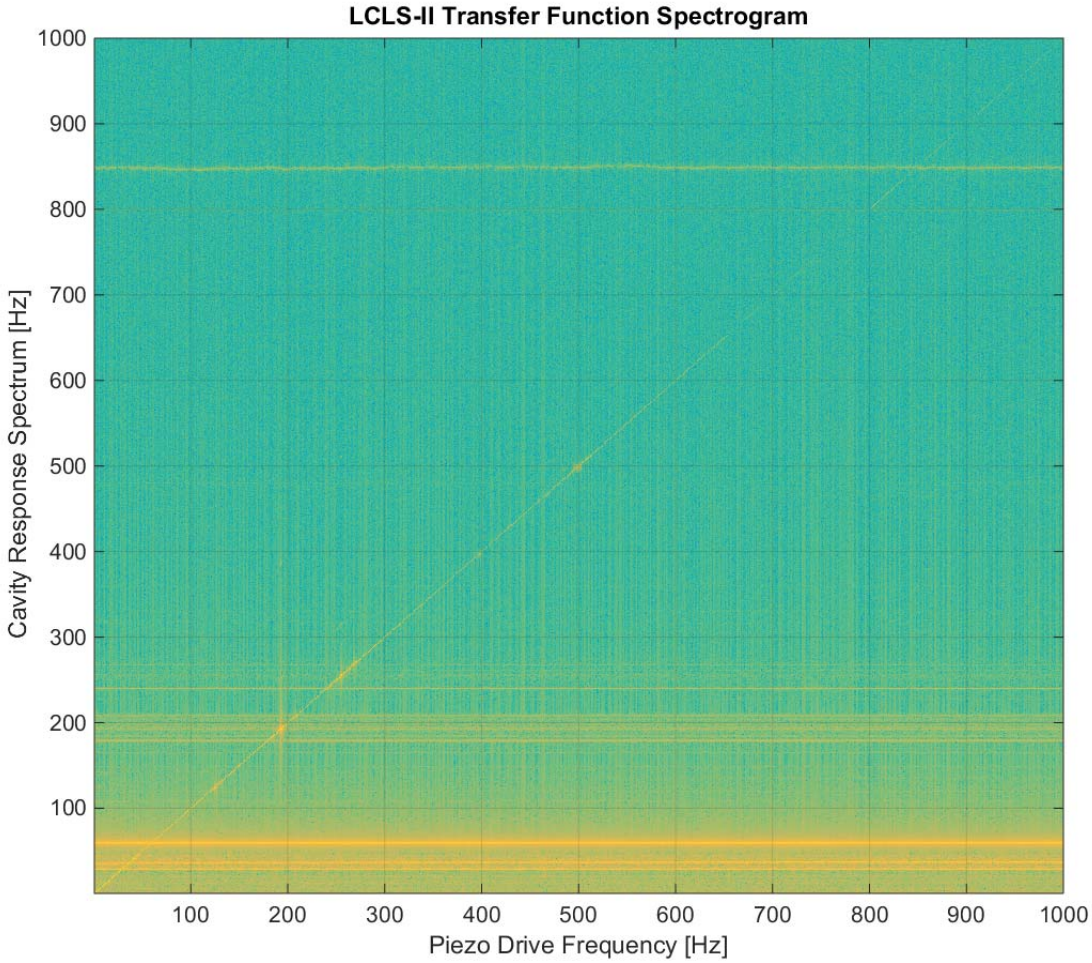


Proportional Detuning Compensation

- Using Forward, Reverse, and Probe signals, detuning is calculated on the fly
- This is filtered, then fed into the piezo with some gain to try and maintain zero detuning
- Data can be sampled and captured at full FPGA clock speed for approximately 10 ms or decimated for longer data sets
- Targeted frequency compensation has been demonstrated

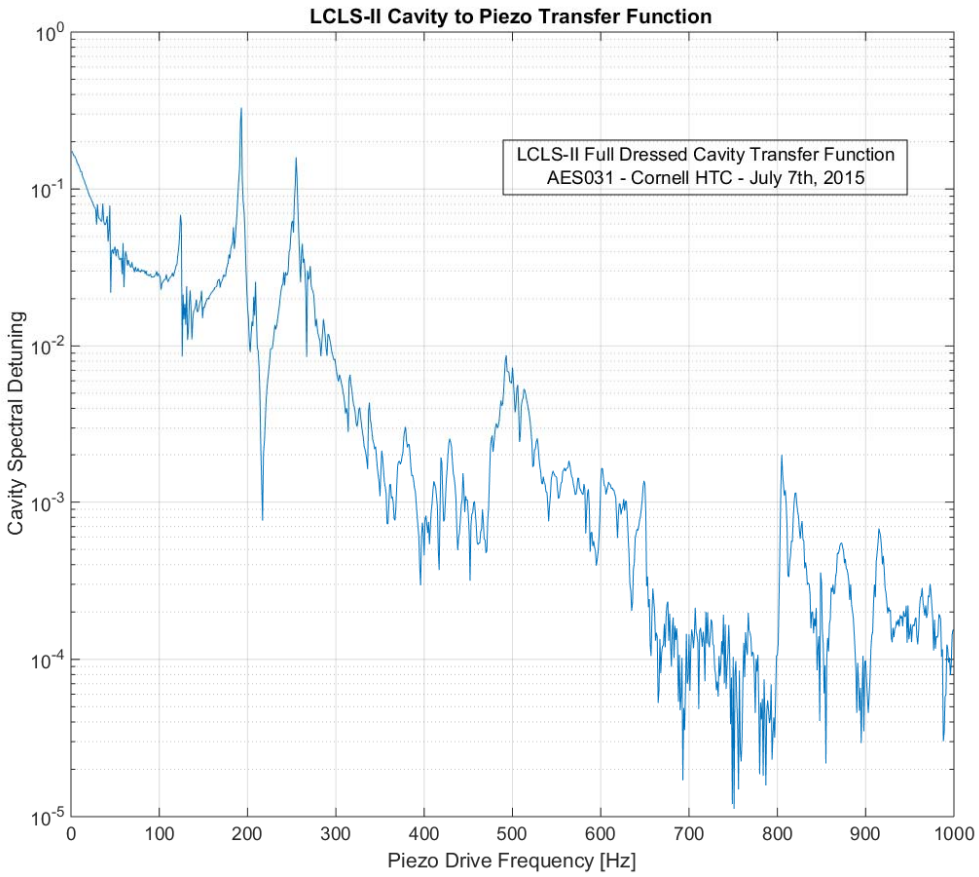


Transfer Function Spectrogram

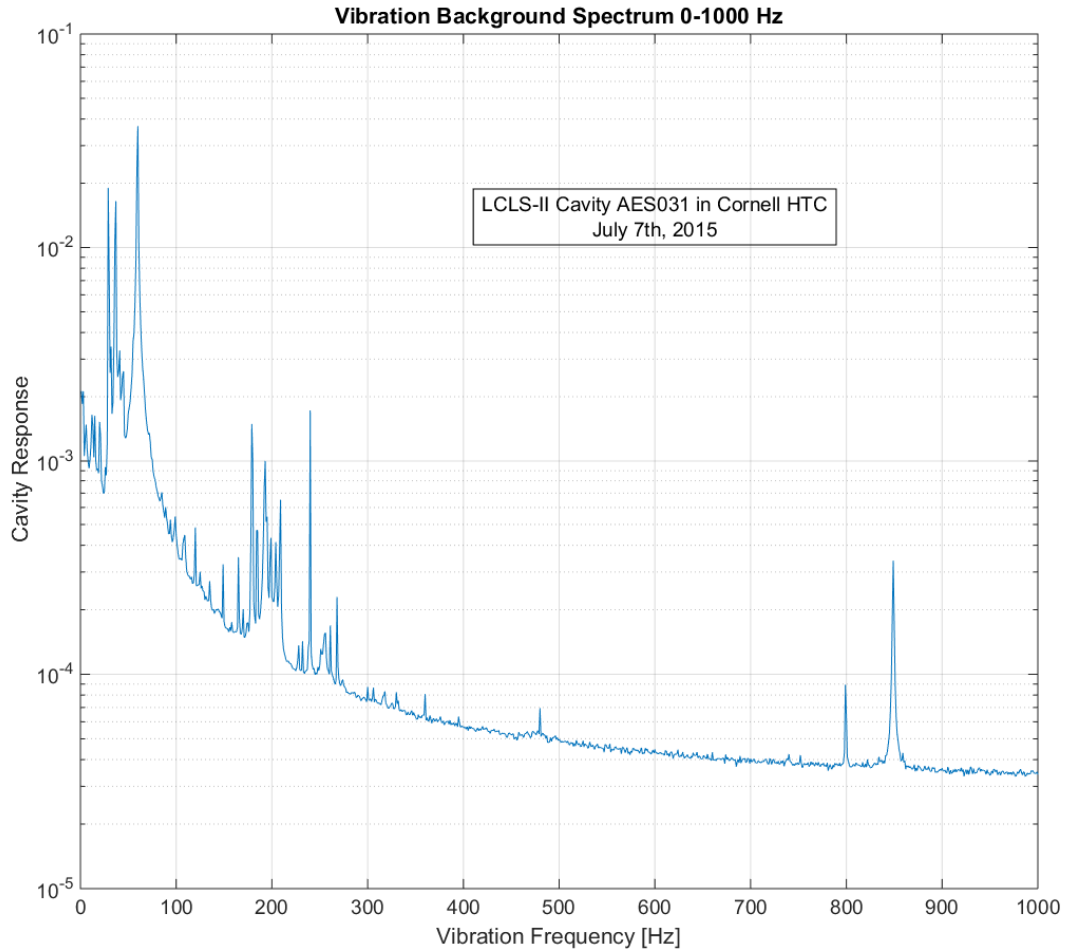


Transfer Function – Cavity Characterization

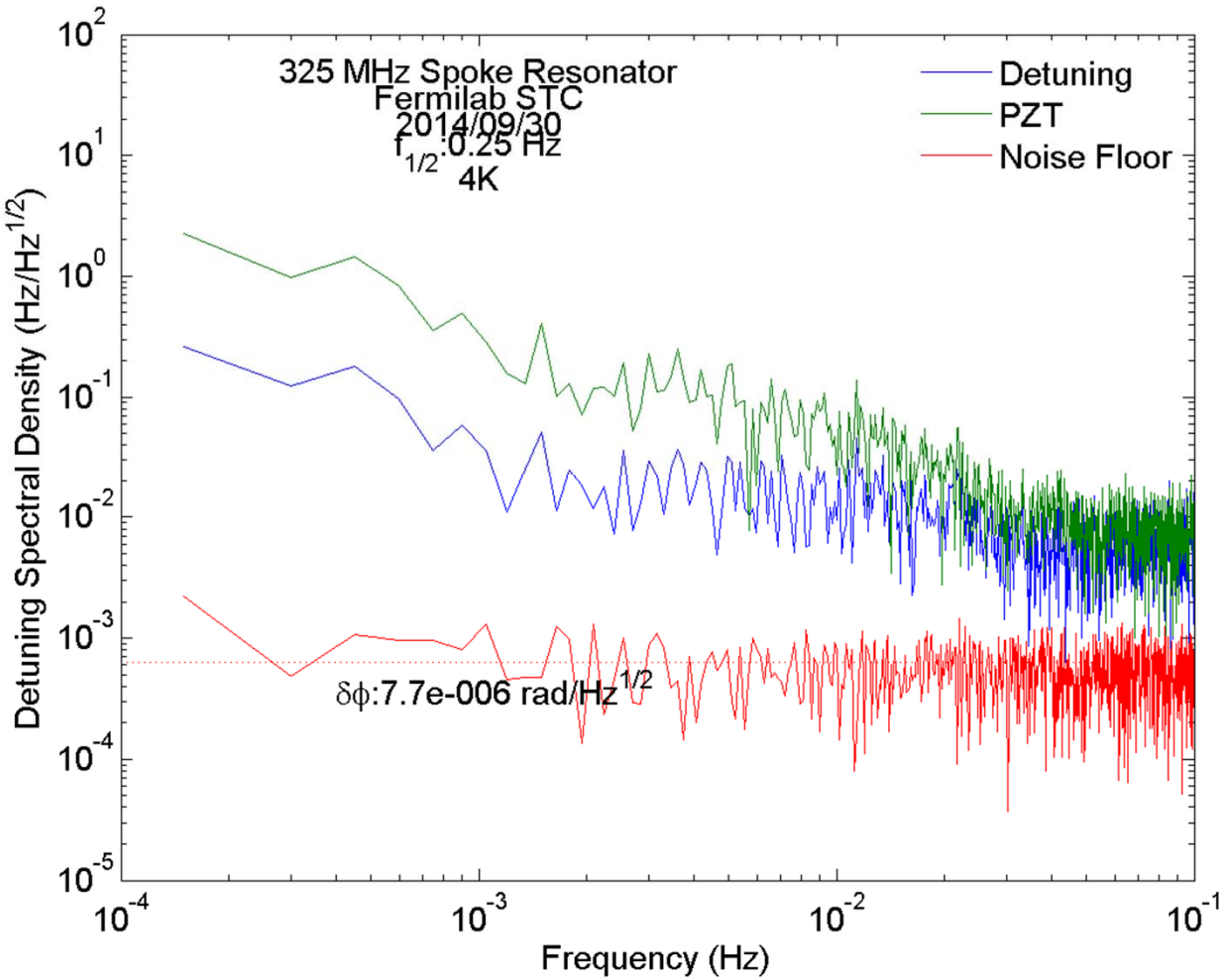
- Further development of advanced controllers requires the ability to characterize the cavity tuner system
- Measurement of the piezo-cavity transfer function is one part of the equation
- Amplitude modulation while the resonance is stabilized is the other
- Both capabilities have been demonstrated in our firmware



Vibrational Backgrounds



Summary

- We continue to work with both analog and digital issues
- Cleanliness/level of analog signals is something we routinely struggle with
- Dynamic range of our ADC/DACs plays a major factor
- Firmware development is a long and arduous process, but we've made significant progress in demonstrating functionality
  - Demonstration of functionality
  - Robustness of these features under different operating conditions
  - Stability of overall code as it expands
- Full simulator is still in construction

Phase Noise Measurement